Features

- **EE Programmable 524,288 x 1- and 1,048,576 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **In-System Programmable via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT6000, AT40K FPGAs, Altera FLEX® Devices, Lucent ORCA® FPGAs, Xilinx XC3000, XC4000, XC5200, SPARTAN® and Virtex® FPGAs**
- **Cascadable Read Back to Support Additional Configurations or Future Higher-density Arrays**
- **Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available in PLCC Package (Pin-compatible Across Product Family)**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Available in 3.3V ± 10% LV and 5V ± 5% C Versions**
- **System-friendly READY Pin**
- **Low-power Standby Mode**

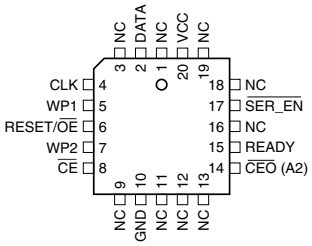
Description

The AT17C512/010 and AT17LV512/010 (high-density AT17 Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17 Series is packaged in the popular 20-pin PLCC. The AT17 Series family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17 Series organization supplies enough memory to configure one or multiple smaller FPGAs. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices also support a write protection mode and a system-friendly READY pin, which signifies a "good" power level to the FPGA and can be used to ensure reliable system power-up.

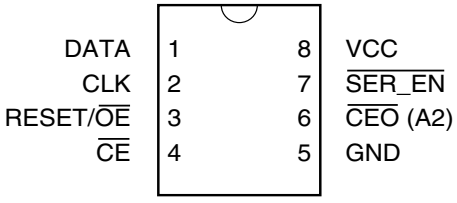
The AT17 Configurator Series can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

Pin Configurations

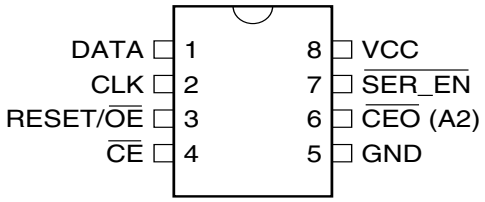
20 PLCC



8 LAP



8 PDIP



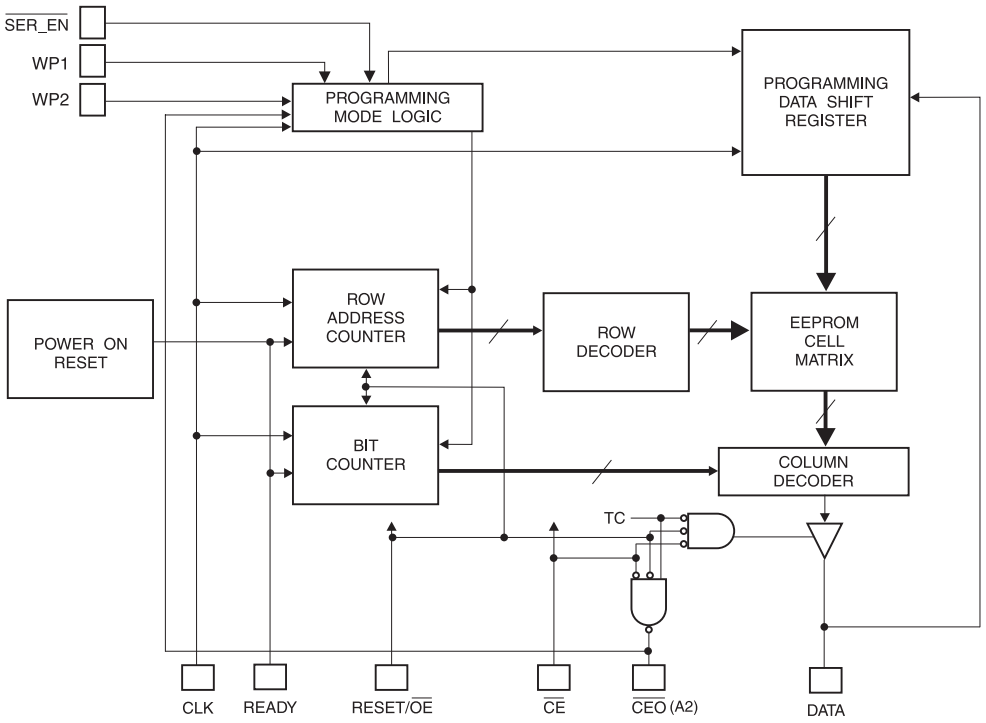
FPGA Configuration EEPROM Memory

512K and 1M

AT17C512
AT17LV512
AT17C010
AT17LV010

Rev. 0944D–06/01

Block Diagram



FPGA Master Serial Mode Summary

The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The AT17 Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

This document discusses the AT40K FPGA interface. For more details or AT6000 FPGA applications, please reference “AT40K Series Configuration” or “AT6000 Series Configuration” application notes.

Controlling the High-density AT17 Series Serial EEPROMs During Configuration

Most connections between the FPGA device and the AT17 Serial Configuration EEPROM are simple and self-explanatory:

The DATA output of the AT17 Series Configurator drives DIN of the FPGA devices.

The master FPGA CCLK output drives the CLK input of the AT17 Series Configurator.

The $\overline{CEO}$ output of any AT17C/LV512/010 drives the $\overline{CE}$ input of the next AT17C/LV512/010 in a cascade chain of EEPROMs.

$\overline{SER\_EN}$ must be connected to VCC (except during ISP).

The READY pin is available as an open-collector indicator of the device’s reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete. This pin is not available in the 8-pin package.

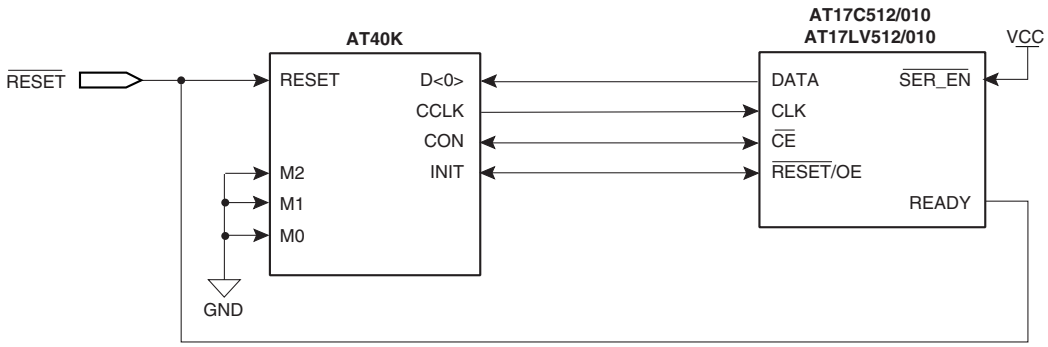
There are two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$.

Condition 1

The simplest connection is to have the FPGA $\overline{CON}$ pin drive both $\overline{CE}$ and RESET/$\overline{OE}$[1] in parallel. Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17 Series Configurator does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Note: 1. For this condition, the reset polarity of the EEPROM must be set active High.

Figure 1. Condition 2 Connection



Notes: 1. Use of the READY pin is optional. The READY pin is not available in the 8-pin DPDIP/SOIC package.
2. Reset polarity of EEPROM must be set active Low.

Condition 2

The FPGA $\overline{CON}$ output drives only the $\overline{CE}$ input of the AT17 Series Configurator, while the RESET/$\overline{OE}$ input is driven by the FPGA INIT pin (Figure 1). This connection works under all normal circumstances, even when the user aborts a configuration before $\overline{CON}$ has gone high. A Low level on the $\overline{RESET}$/OE[1] input – during FPGA reset – clears the Configurator's internal address pointer, so that the reconfiguration starts at the beginning.

Note: 1. For this condition the reset polarity of the EEPROM must be set active Low.

The AT17 Series Configurator does not require an inverter for either condition since the RESET polarity is programmable.

Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory.

As the last bit from the first Configurator is read, the clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line driver. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded Configurators are reset if the RESET/$\overline{OE}$ on each Configurator is driven to its active (default High) level.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ input can be tied to its inactive (default Low) level.

AT17 Series Reset Polarity

The AT17 Series Configurator allows the user to program the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This feature is supported by industry-standard programmer algorithms. For more details on programming the EEPROMs reset polarity, please

reference the “Programming Specification for Atmel’s FPGA Configuration EEPROMs” application note.

Programming Mode

The programming mode is entered by bringing $\overline{\text{SER\_EN}}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at VCC supply only. Programming super voltages are generated inside the chip. See the “Programming Specification for Atmel’s FPGA Configuration EEPROMs” application note for further information. The AT17C parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.3V nominal.

Standby Mode

The AT17C/LV512/010 Series Configurator enters a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. In this mode, the Configurator consumes less than 0.5 mA of current at 5V. The output remains in a high impedance state regardless of the state of the $\overline{\text{OE}}$ input.

Pin Configurations

8 PDIP/ LAP Pin	20 PLCC Pin	Name	I/O	Description
1	2	DATA	I/O	Three-state DATA output for configuration. Open-collector bi-directional pin for programming.
2	4	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
	5	WP1	I	WRITE PROTECT (1). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. See the “Programming Specification” application note for more details.
3	6	RESET/$\overline{\text{OE}}$	I	RESET/Output Enable input (when $\overline{\text{SER\_EN}}$ is High). A Low level on both the $\overline{\text{CE}}$ and RESET/$\overline{\text{OE}}$ inputs enables the data output driver. A High level on RESET/$\overline{\text{OE}}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{\text{OE}}$ or $\overline{\text{RESET}}$/OE. This document describes the pin as RESET/$\overline{\text{OE}}$.
	7	WP2	I	WRITE PROTECT (2). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. See the “Programming Specification” application note for more details.
4	8	$\overline{\text{CE}}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will not enable/disable the device in the 2-wire Serial Programming Mode (i.e., when $\overline{\text{SER\_EN}}$ is Low).
5	10	GND		Ground pin. A 0.2 µF decoupling capacitor between VCC and GND is recommended.

Pin Configurations (Continued)

8 PDIP/ LAP Pin	20 PLCC Pin	Name	I/O	Description
6	14	$\overline{CEO}$	O	Chip Enable Output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter, $\overline{CEO}$ will stay High until the entire EEPROM is read again.
		A2	I	Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{SER\_EN}$ is Low; see the “Programming Specification” application note for more details).
	15	READY	O	Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (Recommend a 4.7 kΩ pull-up on this pin if used). The DIP/SOIC package.
7	17	$\overline{SER\_EN}$	I	Serial enable must be held High during FPGA loading operations. Bringing $\overline{SER\_EN}$ Low enables the 2-wire Serial Programming Mode.
8	20	VCC		+3.3V/+5V power supply pin.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		AT17CXXX Min	AT17CXXX Max	AT17LVXXX Min	AT17LVXXX Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	3.0	3.6	V

DC Characteristics

V_{CC} = 5V ± 5% Commercial/5V ± 10% Industrial/Military

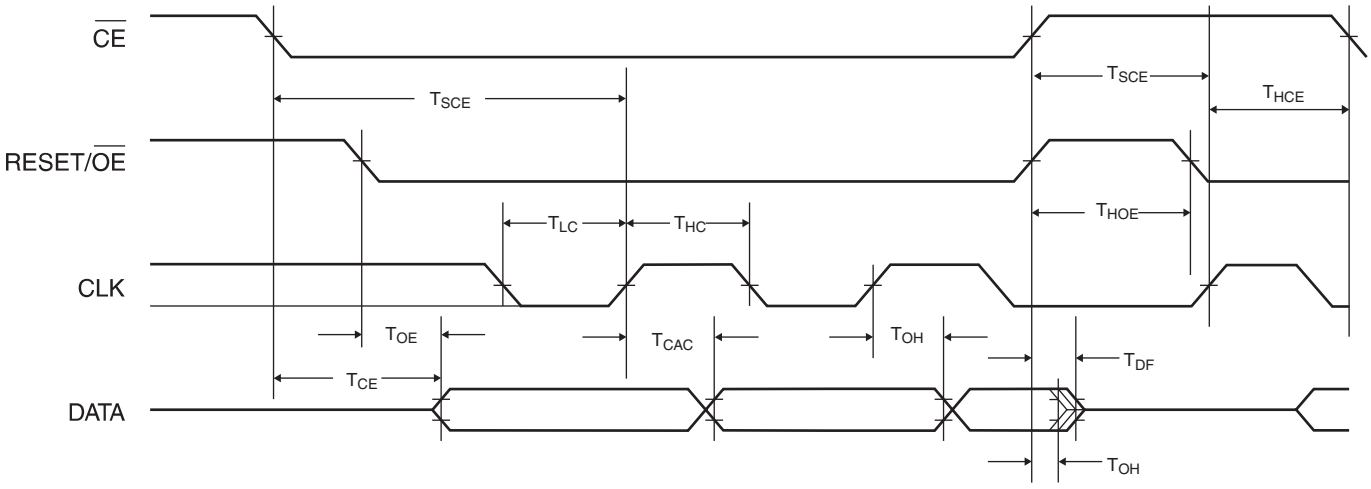
Symbol	Description		Min	Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0.0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply Current, Active Mode			10.0	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10.0	10.0	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		0.5	mA
		Industrial/Military		0.5	mA

DC Characteristics

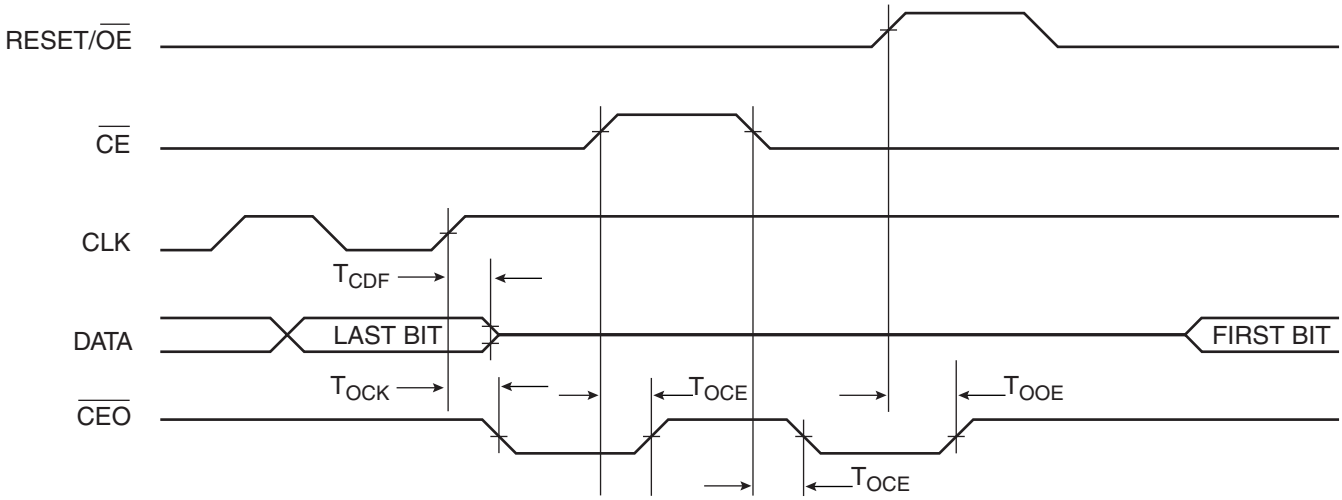
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0.0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply Current, Active Mode			5.0	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10.0	10.0	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		100.0	µA
		Industrial/Military		100.0	µA

AC Characteristics



AC Characteristics When Cascading



AC Characteristics for AT17C512/010

V_{CC} = 5V ± 5% Commercial/V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		30.0		35.0	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		45.0		45.0	ns
T_{CAC}[2]	CLK to Data Delay		50.0		50.0	ns
T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0.0		0.0		ns
T_{DF}()	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50.0		50.0	ns
T_{LC}	CLK Low Time	20.0		20.0		ns
T_{HC}	CLK High Time	20.0		20.0		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	20.0		25.0		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0.0		0.0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter Is reset)	20.0		20.0		ns
F_{MAX}	MAX Input Clock Frequency	15.0		15.0		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

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AC Characteristics for AT17C512/010 When Cascading

V_{CC} = 5V± 5% Commercial/V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50.0		50.0	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		35.0		40.0	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		35.0		35.0	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		30.0		30.0	ns
F_{MAX}	MAX Input Clock Frequency	12.5		12.5		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

AC Characteristics for AT17LV512/010

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		50.0		55.0	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		55.0		60.0	ns
T_{CAC}[2]	CLK to Data Delay		55.0		60.0	ns
T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0.0		0.0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50.0		50.0	ns
T_{LC}	CLK Low Time	25.0		25.0		ns
T_{HC}	CLK High Time	25.0		25.0		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	30.0		35.0		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0.0		0.0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	25.0		25.0		ns
F_{MAX}	MAX Input Clock Frequency	15.0		10.0		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels

AC Characteristics for AT17LV512/010 When Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50.0		50.0	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		50.0		55.0	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		35.0		40.0	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		35.0		35.0	ns
F_{MAX}	MAX Input Clock Frequency	12.5		10.0		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

Ordering Information – 5V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17C512-10JC AT17C512-10PC AT17C512-10CC	20J 8P3 8C	Commercial (0°C to 70°C)
	AT17C512-10JI AT17C512-10PI AT17C512-10CI	20J 8P3 8C	Industrial (-40°C to 85°C)
1M	AT17C010-10JC AT17C010-10PC AT17C010-10CC	20J 8P3 8C	Commercial (0°C to 70°C)
	AT17C010-10JI AT17C010-10PI AT17C010-10CI	20J 8P3 8C	Industrial (-40°C to 85°C)

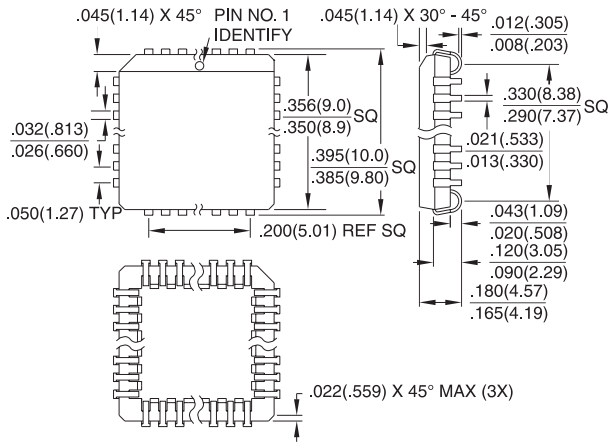
Ordering Information – 3.3V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17LV512-10JC AT17LV512-10PC AT17LV512-10CC	20J 8P3 8C	Commercial (0°C to 70°C)
	AT17LV512-10JI AT17LV512-10PI AT17LV512-10CI	20J 8P3 8C	Industrial (-40°C to 85°C)
1M	AT17LV010-10JC AT17LV010-10PC AT17LV010-10CC	20J 8P3 8C	Commercial (0°C to 70°C)
	AT17LV010-10JI AT17LV010-10PI AT17LV010-10CI	20J 8P3 8C	Industrial (-40°C to 85°C)

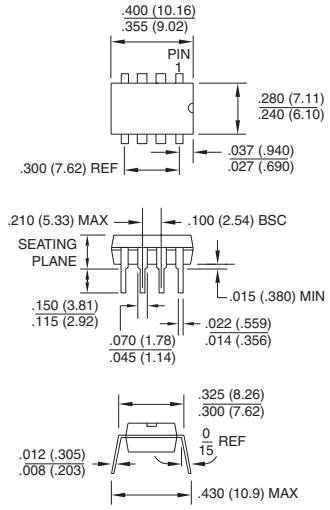
Package Type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
8P3	8-lead, Plastic Dual Inline Package (PDIP)
8C	8-lead, leadless Aray package (LAP)

Packaging Information

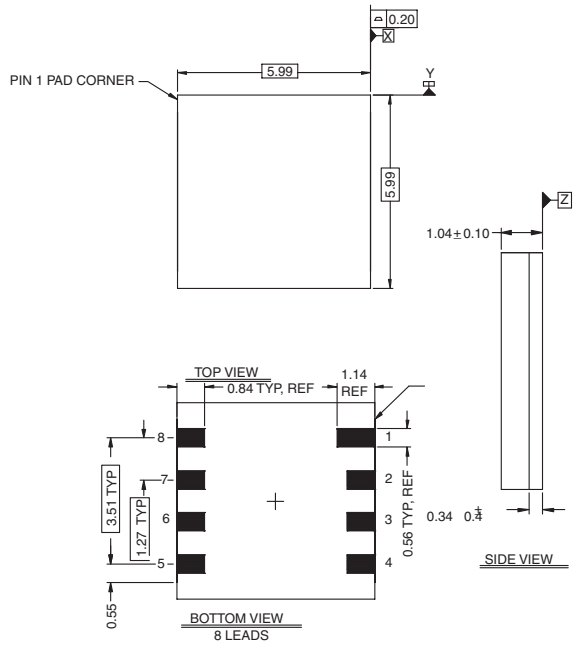
20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



8P3, 8-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



8C, 8-lead, (6mm x 6mm), Leadless Array Package (LAP)
Dimensions in Millimeters



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